COURSE CODE	COURSE NAME	L-T-P-C	YEAR OF INTRODUCTION
EC206	Computer Organisation	3-0-0-3	2016

Prerequisite: EC207 Logic circuit design

Course objectives:

- To impart knowledge in different aspects of processor design.
- To develop understanding about processor architecture.
- To impart knowledge in programming concepts.
- To develop understanding on I/O accessing techniques and memory structures.

Syllabus:

Functional units of a computer, Arithmetic Circuits, Processor architecture, Instructions and addressing modes, Execution of program, micro architecture design process, design or data path and control units, I/O accessing techniques, Memory concepts, memory interface, cash and virtual memory concepts

Expected outcome:

The student should be able to:

- Illustrate the structure of a computer
- Categorize different types of memories
- Explain various techniques in computer design.

Text Books:

1. David Money Harris, Sarah L Harris, Digital Design and Computer Architecture, Morgan Kaufmann – Elsevier, 2009

References:

1. William Stallings: "Computer Organisation and Architecture", Pearson Education.
2. John P Hayes: "Computer Architecture and Organisation", Mc Graw Hill.
3. Andrew S Tanenbaum: "Structured Computer Organisation", Pearson Education.
4. Craig Zacker: "PC Hardware : The Complete Reference", TMH.
5. Carl Hamacher : "Computer Organization ", Fifth Edition, Mc Graw Hill.
6. David A. Patterson and John L. Hennessey, "Computer Organisation and Design", Fourth Edition, Morgan Kaufmann.

Course Plan

Module	Course content (42 hrs)	Hours	Sem. Exam Marks
I	Functional units of a computer: Arithmetic Circuits – Adder- Carry propagate adder, Ripple carry adder, Basics of carry look ahead and prefix adder, Subtractor, Comparator, ALU	4	15
	Shifters and rotators, Multiplication, Division	3	
	Number System- Fixed Point & Floating Point	1	
II	Architecture – Assembly Language, Instructions, Operands – Registers, Register set, Memory, Constants	2	15
	Machine Language –R-Type, I-Type, J-Type Instructions, Interpreting Machine Language code	3	
FIRST INTERNAL EXAM			

III	Addressing Modes – register only, immediate, base, PC-relative, Pseudo – direct	3	**15**
	Steps for Executing a Program – Compilation, Assembling, Linking, Loading	3	
	Pseudoinstuctions, Exceptions, Signed and Unsigned Instructions, Floating Point Instructions	3	
IV	Microarchitecture- design process	2	**15**
	Single cycle processor, Single cycle data path, single cycle control	2	
	multi cycle processor, multi cycle data path, multi cycle control	3	
SECOND INTERNAL EXAM			
V	Memory & I/O systems – I/O accessing techniques: programmed, interrupt driven and DMA, DMA bus arbitration	3	**20**
	Memory Arrays – Bit Cells, Organization, Memory Ports Memory types- DRAM, SRAM, Register Files, ROM	3	
VI	Memory - Hierarchy, Performance analysis	1	**20**
	Cache Memory – direct mapped, multi way set associate cache, Fully associate cache	3	
	Virtual Memory – Address Translation, Page Table, Translation Look aside Buffer, Memory Protection, replacement polices	3	
END SEMESTER EXAM			

Question Paper Pattern

The question paper consists of three parts. Part A covers modules I and II, Part B covers modules III and IV and Part C covers modules V and VI. Each part has three questions. Each question can have a maximum of four subparts. Among the three questions one will be a compulsory question covering both the modules and the remaining two questions will be as one question from each module, of which one is to be answered. Mark pattern is according to the syllabus with maximum 50 % for theory and 50% for logical/numerical problems, derivation and proof.